Application Note 60

TMC2068P7C Demonstration Board

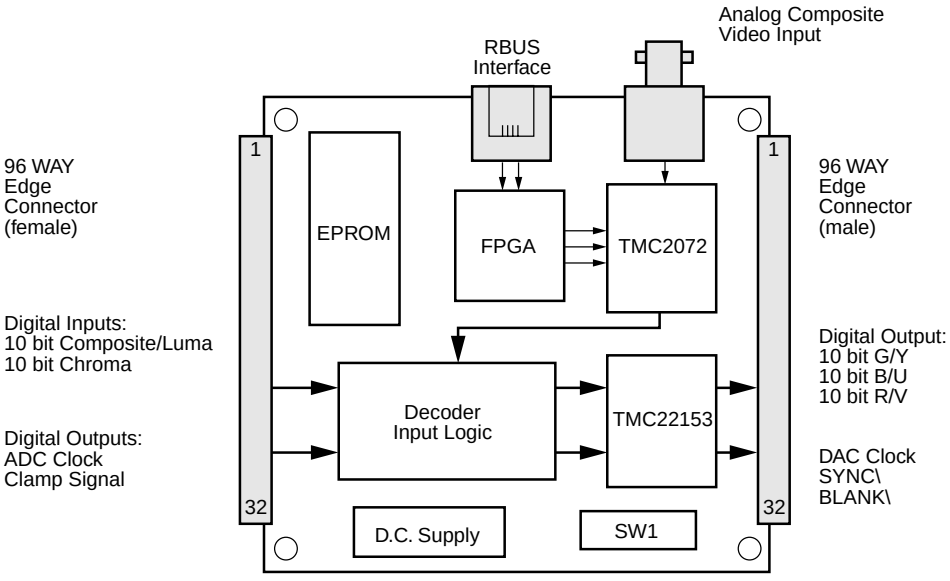
The TMC2068P7C decoder demonstration board provides a flexible base for evaluating the performance of the TMC22153 10 bit digital decoder. The TMC22071A provides the clocks and HSYNC and VSYNC signals required to lock the TMC22153 to either the 10 bit Y/COMP and CHROMA signals from the edge connector or to the 8 bit output from the TMC22071A. The selection of the decoder input is controlled by the jumpers E2 and JP3.

The FPGA is configured by the EPROM when the FPGA-PGM switch is depressed, once the FPGA has been programmed the TMC22153 and TMC22071A are programmed when the DEV-PGM button is depressed, using register and XLUT maps stored within the EPROM. The different PAL and NTSC maps are selected by the S3 DIP switch. This second programming stage is not necessary if the RBUS interface is connected, in which case the RBUS serial interface signals are connected directly to the RBUS port of the TMC22153 and the FPGA. The FPGA holds the TMC22071A register map and programs the TMC22071A automatically after being updated.

The control pins of the TMC22153 are connected to a DIP switch, SW1. These switches control the BUFFER, MASTER[1:0], SER\, SA[2:0] functions.

The output of the board is configured to allow 10 bit G/Y, B/U, or R/V outputs through a standard 96 way edge connector for connection to the TMC2069P7C triple DAC demonstration board. The position of the R/V can be moved to the G/Y output for direct connection to the Genesis Microsystems DICE demonstration board.

A 72 pin header is provided between the VIDEOA and VIDEOB ports of the TMC22153 allowing external field or frame stores to be designed and debugged. When using the header the COVER[0:9] output on U10 needs to be disabled as the header output is also connected the COVER[0:9] data bus.



TMC22153 Digital Decoder demonstration board

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